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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/055,568	01/22/2002	Mou-Shiung Lin	MEGP0004USA	6093

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION
P.O. BOX 506
MERRIFIELD, VA 22116

EXAMINER

MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
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2813

NOTIFICATION DATE	DELIVERY MODE
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06/26/2009

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 10/055,568	Applicant(s) LIN ET AL.	
	Examiner JAMES M. MITCHELL	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 February 2009.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 219-223,228,232,236,238-242,250-257,259,260 and 262-267 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 219-223,228,232,236,238-242,250-257,259,260 and 262-267 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>3/27/2009</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This office action is in response to applicant's remarks filed February 26, 2009.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on March 27, 2009 was in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 219-223,228,232,236,238-242,250-257,259,260 and 262-267 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsai (U.S. 6,180,445)¹ in combination with Korman (U.S. 5,959,357).

Tsai discloses: (Fig.) discloses:

(cl. 219, 264) A chip package comprising: one silicon die (10, Col. 1, Lines 9-11) having a first top surface at a horizontal level; a first insulating layer (15, 23) over said horizontal level, over said only one die, ~~and across an edge of said only one die,~~ wherein said first insulating layer comprises comprising a first portion over said only one die and a second portion over said substrate but not over said only one die; a patterned circuit layer (19) over said first insulating layer, over said horizontal level, over said only one die and over said substrate, wherein said patterned circuit layer is connected (via 17) to said only one die through a first opening in said first insulating layer, an inductor (22) over said horizontal level and over said first insulating layer; and a second insulating layer (42) on said inductor;

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(cl.223) said patterned circuit layer connects multiple portions of said only one die through said first opening and through a second opening in said first insulating layer (e.g. electrical connection thorough 17 to die therefore electrically conductive vias are formed);

(cl. 228) wherein said first insulating layer comprises polyimide (Abstract);

(cl. 251, 252) said substrate has a second top surface (23) is coplanar/ over with first surface (e.g. 15);

¹ In anticipation of an amendment or RCE note that newly cited Sugaya (U.S. 6,538,210) in e.g. Fig. 14

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(cl. 260) and solder bumps (46);

(cl. 263) multiple active devices in a chip (IC). Tsai does not show an adhesive

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material joining said substrate and said only one die.

However, Korman discloses attaching a die to a substrate (24 with a thermally conductive paste (e.g. to provide heat dissipation).

It would have been obvious to one of ordinary skill in the art to incorporate forming a metal substrate (22) on the die of Tsai in order to provide a heat dissipation as taught by Korman (Col. 4, Lines 55-56)

With respect to claim 220 that circuit layer comprises a second trace having a thickness greater than that of said first trace. Applicant has not disclosed that the dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. As such, the selected dimensions would have been obvious, since it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

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With respect to the intended use limitation of claim 221, 222, 239 that the circuit layer comprises a power bus, the product is the same as claimed and therefore capable

further evidences lack of novelty or nonobviousness. Not only does Sugaya anticipate the claimed

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of performing in the same manner. The claim is unpatentable, since it has been held that the manner in which a claimed apparatus is intended to be employed does not differentiate the claimed apparatus from a prior art apparatus satisfying the claimed structural limitations. *Ex parte Masham*, 2 USPQ2d 1647 (1987).

With respect to the claim 232, 253, 255, 259, 226, 267, that said first insulating layer comprises benzocyclobutene (BCB), the the first and second layers have different materials or metals, or polymer is an epoxy, examiner takes official notice that BCB as an insulating material in ILD and polymer epoxies for protection or gold bumps, copper used for inductors are known in the art. As such, its selection would have been obvious to one of ordinary skill in art. See MPEP 2144.07.

With respect to use of alternate adhesive being a tape, Examiner takes official notice that tapes are known in the art for securing chip (e.g. lead on chip, & Lead under chip packaging). As such the use of tapes would have been obvious to one of ordinary skill in the art to provide an alternate attachment means.

Moreover, because use of tapes is one of a finite methods to solve the problem attaching materials, it would have been obvious to one of ordinary skill in the art to pursue tapes as an attachment means. See e.g., *KSR Int'l v. Teleflex Inc.*, 127 S.Ct. 1727, 1743, 550 U.S. 17 (2007) (finding that when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within

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invention, but it shows the same embodiment disclosed by applicant.

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his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense).

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With respect to the process limitation of claims 239, 240 and 265 that the circuit is patterned and electroplated or sputtered. The prior art forms the same structure as claimed. The limitation does not impart patentability. See e.g. "[E]ven though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process." In re Thorpe, 777 F.2d 695, 698, 227 USPQ 964, 966 (Fed. Cir. 1985).

With respect to claim 241, 242 that the inductor and bump not have a portion over the die. This amounts to nothing more than an arrangement of parts. Applicant has not disclosed that such an arrangement produces unexpected results or is critical. As such, the rearrangement could have been obvious to one of ordinary skill in the art. See In re Japikse, 181 F.2d 1019, 86 USPQ 70 (CCPA 1950) (Claims to a hydraulic power press which read on the prior art except with regard to the position of the starting switch were held unpatentable because shifting the position of the starting switch would not have modified the operation of the device.); In re Kuhle, 526 F.2d 553, 188 USPQ 7 (CCPA 1975) (the particular placement of a contact in a conductivity measuring device was held to be an obvious matter of design choice).

With respect to the shape of the substrate having a recess in claim 250, 257, applicant has not disclosed that his shape are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. As such, the selected dimensions would have been obvious to one of ordinary skill in the art to select the claimed dimensions, since it has been held that the selected dimensions are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

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Response to Arguments

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Applicant's arguments filed February 26, 2009 have been fully considered but they are not persuasive. Applicant contends that his invention is patentable, because allegedly Tsai's substrate, 10 is not a die. Applicant rightfully contends that a die is "a small piece cut from a semiconductor wafer along scribes lines". The USPTO's classification definition defines a die as a "[a] tiny piece of semiconductor material, separated from a semiconductor slice, on which one or more active electronic components are formed". Because item 10 is silicon and therefore semiconductor material cut from a wafer on which active components are formed as evidenced by devices formed in active region 44 of Tsai, it meets the broad definition of a die.

Applicant also contends that his invention is patentable, because the first insulating layer of Tsai is not across or over the die, but in the die. Examiner

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respectfully disagrees. Applicant's own reference filed February 26, 2009 via Tummala ("Packaging Handbook) on page 82 calls for a multilayer "wiring have been created **on the chip** [also known as a die]" **[Emphasis added]**. Multilayer wiring disclosed in Tummala (See Fig. 8-2) comprises ILD in the same manner as Tsai first insulating layers. Because Tsai also discloses an ILD over a tiny piece of semiconductor with active devices formed thereon in a like manner, the ILD can be reasonably interpreted as also being **on the chip/die**. Applicant's remarks amount to mere conjecture and are insufficient to overcome examiner's prima facie case of obvious. See MPEP 2145 (In re Geisler, 116 F.3d 1465, 43 USPQ2d 1362 (Fed. Cir. 1997) ("An assertion of what seems to follow from common experience is just attorney argument and not the kind of factual evidence that is required to rebut a prima facie case of obviousness.")). For the reasons stated above, examiner's rejection is maintained.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art discloses use of passive components formed over chips/dies.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES M. MITCHELL whose telephone number is (571)272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mathew Landau can be reached on (571) 272-1731. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Deleted: THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). ¶
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action. ¶

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

June 6, 2009
/James M. Mitchell/
Examiner, Art Unit 2813